mDOM DAQ & ICM Preliminary Design Review

26-27 August 2019, DESY Zeuthen, Germany

Scope of review

Reviewers were charged with evaluating the mDOM DAQ Electronics (WBS 1.3.1.1), high voltage subsystem (WBS 1.3.1.3), and Ice Communications Module (ICM) (WBS 1.3.4) at the level of a preliminary design. This roughly means that at least a prototype exists, has been verified to meet design requirements (or at least any deviation is understood), and there is a plan for building first production articles substantially similar to the prototype. Full requirements are detailed in the Design Flow document, linked below. Some comments below may fall somewhat outside of this scope, dealing with interfaces to other mDOM parts or to the CPT (Cables, Power, and Timing) system.

Reviewers:
Michael DuVernois (UW-Madison, WIPAC), Andrew Laundrie (UW-Madison, PSL), Brian Ferguson (Michigan State University), and Matthias Kleifges (Karlsruhe Institute of Technology).

Presentation materials:
https://drive.google.com/drive/folders/1LmIzRq2hAP5MzM4ZQhTHTHeMwx4Yg6Nh?usp=sharing

Design flow guide:
https://drive.google.com/open?id=1jOn3k4E0YYGZusg7phDEUbHs1YXgWe9u

Action item list (for a broader list of folks):
https://docs.google.com/spreadsheets/d/12jOviouZ9G1KcEe7omOPA1XkHgtc6z43ZrDXfVoSi9U/edit?usp=sharing

Executive summary

The review committee finds that the mDOM electronics is progressing well, the basic designs seem reasonable, and no show stoppers were identified. The next 12-18 months will see delivery of ICM units for the first D-Egg production batch, mini-FieldHubs for D-Egg design verification, the final design review of the high voltage boards to allow for PMT procurement and integrated PMT+HV manufacture, the final design review of the mDOM mainboard electronics, and the start of mDOM production. In parallel, there is the mDOM mainboard firmware, the ICM firmware, testing of communications over the Upgrade in-ice cable, and testing locally, at the Northern Test System, and at Chiba with the D-Eggs. There is a lot going on. The committee has some higher level recommendations associated with scheduling and design choices, and then more detailed comments, questions, and suggestions divided up by technical topic below.

High-level recommendations

1. Produce a list of milestones for the near-term mDOM & ICM design development. Include the decision points (e.g., AC vs. DC coupling, how the bases and PMTs come together, which PMTs) and deliveries of components (and firmware) to other groups.

2. The engineering team at DESY has a lot of deliverables over the next couple of years, and could use some additional resources. These might be local or contributed remotely. Perhaps some of the test stands or other ancillary deliverables could be outsourced.

3. As much as possible follow the (successful) Gen 1 design, concentrate on changes and improvements, and test them carefully. Don't underestimate the time and manpower required for firmware and software.

4. Carefully consider electrical noise, a problem that can take a long time to isolate, as there are significant pickup possibilities inside the optical module from the HV base as well as communications noise issues arising from cable pickup.

5. Make a plan for which pieces of the firmware are required for various external activities (such as D-Egg design verification) and at what times. Ensure there is a plan to match.

Reviewer comments, questions, and suggestions

1.3.1.1 mDOM Data Acquisition Electronics

Analog Front End (AFE)
The input signal from High Voltage Subsystem is un-terminated on one of the analog front end designs, so AFE must be powered before HV as otherwise its input stage can be damaged. It was discussed that this can occur, so protecting this interface must be a priority. Any such protection should be capable of safely absorbing the maximum stored energy in the HV supply. In particular, in a power-disconnect situation, the high-voltage is likely to be present on the PMTs after the AFE has been turned off. Although the HV base includes a voltage limiter on the output, it may not provide adequate protection for the AFE.

The power consumption has been measured as 140mW/channel before FPGA, and of that 88mW/chan are for the ADC. There is about 11MHz of bandwidth at the back end of the AFE. A testboard has been employed for studying the AFE and digitizer chain.

It was very good to see the resistor / capacitor variability and temperature analysis. The parts selection variation is expected to yield +/-8% amplitude variation from the resistors and about 1.5% from the capacitors. Built in test equipment (BITE), a pair of signal generators switched

into the AFE signal chain, allow for a more precision calibration (<1%). The inclusion and design of on-board calibration circuits (test pulser) is excellent; well done.

There are a couple of plots which might be useful to show system performance: a plot of trigger efficiency versus amplitude (or charge), and the pulse pair efficiency as a function of both pulse separation time and trigger level. Also the ADC to charge conversion doesn't quite fit together yet, this would be a good check on the system performance as well.

Firmware (FW)
The firmware design is in a very early state. It seems as though there are conflicting desires within the team as to how the firmware should be designed. It is recommended that a plan for future development be formalized. In particular, which parts of the firmware development have priority, should be determined.

Mainboard (MB)
mDOM mainboard Engineering Requirements Document (ERD) states that the noise requirement is 1/50 pe, but the AFE is designed with a noise floor of ⅕ pe. Is this simply a typo, does the mDOM not meet a physics requirement, or is the requirement wrong?

The primary mainboard (TRACO) power module's start-up behavior with a long twisted pair should be tested. Transmission line effects can induce oscillation. And if there are two series soft-starts, how do those work together/interact?

Recommendations:

1. The choice between the various designs, and AC or DC coupling should be made as soon as it is practical to do so.
2. Other mainboard requirements such as reliability and unbrickability need to be explored.
3. Test the mainboard and ICM with a cable as soon as possible.
4. Clarify the noise requirements.

1.3.1.3 mDOM High Voltage Subsystem

The impact of the EMI from the MicroBase is unknown. It is known from gen1 experience that RAPCAL is very sensitive to EMI, so it would be a good idea to test the effect of the MicroBase on the ICM when RAPCAL is being run. It is also worth testing how sensitive the MicroBase is to interference from other nearby MicroBases.

The MicroBase has been tested up to 3000V (with a limiter diode removed), at which point it sparked. It would be good to determine at what voltage arcing occurs in ½ atmosphere, and also at what point arcing occurs between adjacent bases mounted on PMTs in the mDOM support structure. It is noted that low pressure tests with the HV subsystem are planned for October 2019.

Conformal coating for the MicroBase should be considered as a risk reduction. Perhaps this could be investigated as part of corona discharge testing. Conformal coating could be limited to problem areas such as underneath and around C19 to increase dielectric strength locally.

It is not clear where the design rules for high-voltage layout originated. Is there an IPC or similar standard being followed?

Where possible, designers should recognize potential noise threats and proactively incorporate shielding and filtering to reduce EMI threats. Possible approaches may include on-board shields and filters, and clamp-on ferrite beads applied to coaxial cables.

Recommendations:

1. Operate multiple HV boards in close proximity as soon as possible to test for interference issues such as beat-frequency modulation or control-loop instability.
2. Test at ½ atmosphere for corona. Explore the maximum operating voltage. Consider HiPot testing.
3. Evaluate the use of conformal coating.
4. Make as soon as possible a selection of the PMT manufacturer (HZC or Hamamatsu) and define the procedure for mounting the HV board.
5. Quickly resolve Hamamatsu's reluctance to attach HV boards to PMTs and determine acceptable alternatives.
6. Proactively include shielding and filtering to reduce EMI threats.

1.3.4 Ice Communications Module (ICM)

Fundamentally the ICM design comes from two major drivers: (1) the Gen1 heritage, in particular the cables remain similar, and the communications protocols can remain the same; and, (2) the need for all in-ice devices to use a common communications hardware and software implementation to reduce risk in bringing multiple optical modules and special devices together in the IceCube Upgrade. The ICM is being designed and built by the same team, who built the communications in the Gen1 IceCube.

For Gen 1 DOMs, common-mode rejection on the comms channel was only about 20 dB for in-band frequencies, due to the lack of effective common-mode filtering and limited balance in the coupling transformer and other input circuitry. This resulted in some DOMs being affected by noise sources such as a 50-MHz meteor radar (no longer operating). Consider adding some common-mode filtering to the ICM input channel.

The ICM must be "unbrickable," that is, the firmware must not allow the hardware to become unresponsive. It seems that this relies on having a robustly tested "golden image," so the requisite testing must be planned to be complete before the first ICM is sealed into a DOM. And this image must be available for D-Egg ICMs in early 2020.

It was asserted that the first 100 ICMs will not go through HASS/HALT (Highly Accelerated Stress Screening/Highly Accelerated Life Test) testing; this moves the risk of these units failing to the D-Eggs in which they will be installed, and should be tracked.

The termination scheme failures modes should be worked through; if the terminated module dies, how do the other modules know that one of them needs to terminate? It seems that this must be commanded from the surface. Test if comms works without termination.

Recommendations:

1. The general idea of putting an ICM on a mainboard as soon as possible is a good one.
2. Evaluate filtering options for the ICM.
3. Work through the failure modes of the termination scheme.

General / Cross-topic comments

There are a number of open issues with the larger mDOM design, including the design of the mDOM harness, the HZC vs. Hamamatsu PMT choice, and the optical gel choice (does the D-Egg stiffer gel prevent peel-away at low temperature?). These came up in passing, and are probably not a comprehensive list. Perhaps we could get an update at the collaboration meeting or on a Tech Board call sometime?

Space has been rented near DESY (in Schoenfeld) of about 800 square meters to share with IceCube and CTA. Work will begin next month on setting up the assembly space.

Upcoming critical milestone dates include the July 2020 final design review of the mDOM, and the beginnings of series mDOM production at DESY in January 2021 and at Michigan State in June 2021.

Does the 96VDC downhole voltage level and the resulting maximum power consumption of an optical module constrain the design? We note the 125MSPS ADC is underclocked at 100MSPS, and other design choices may also be dictated by the power available. What is the plan to resolve the delivery voltage?

With PMT / HV base production beginning in six months, it seems imperative that integrated testing (to include at least PMT / HV / Analog Front End) be prioritized. It is very common to learn things during integration testing that result in changes being made to one or both sides of an interface.

Looking through the presented information, it seems that:

ICM - 417 mW (external oscillator could reduce this, firmware might increase it)
AFE (Axel's) - 140 mW x 24
MicroBase - ~20 mW x 24
Total of these components: 4257 mW

Remaining for Mainboard digital (assuming 5W max): 743 mW

Recommendations:

1. Clarify how electrical grounds are handled on the mainboard, cable, and ICM.
2. Are handling requirements, such as ESD protection, defined?
3. Have environmental requirements been established for material storage and handling, such as humidity control and cleanliness?
4. Decide when the downhole string voltage must be known. What are the operational and safety risks in choosing the higher voltage level vs remaining at 96V?
5. Begin integrated testing as soon as possible.
6. An overall power budget should be developed.